REMARKS

The application has been reviewed in light of the final Office Action dated December 17, 2003. Claims 1-39 are pending and presented for reconsideration in this application, with claims 1, 9, 17, 25, 29, 33 and 37-39 being in independent form. By this Amendment, independent claims 1, 9, 17, 25, 29, 33 and 37-39 have been amended to clarify the claimed invention, without narrowing the scope of the claims (i.e. no additional limitations have been added). It is submitted that no new issues and no new matter have been added. Accordingly entry of this Amendment is requested.

Claims 1-39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,943,487 to Messerman et al. in view of U.S. Patent No. 6,324,678 to Dangelo et al. ("Dangelo '678"), and further in view of U.S. Patent No. 5,867,397 to Koza et al., and further in view of the Microsoft Press Computer Dictionary, Third Edition. Claims 1-39 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,535,370 to Raman et al. in view of U.S. Patent No. 5,521,834 to Crafts et al. and further in view of U.S. Patent No. 5,493,508 to Dangelo et al. ("Dangelo '508").

Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claims 1, 9, 17, 25, 29, 33, and 37-39 are patentable over the cited art, for at least the following reasons.

The present application relates to estimation of electric power consumption by integrated circuits which are comprised of basic cells and mega cells. More specifically, the application is directed to tools for estimating electric power consumption by an integrated

circuit which use information collected during logic simulation.

Applicants found that power consumption of an integrated circuit can be more accurately estimated by estimating electric power consumed by mega cells of the integrated circuit based on the logic simulations and pre-established power consumption data, in addition to estimating electric power consumed by basic cells of the integrated circuit. The application describes (at, for example, pages 8-15) techniques for estimating electric power consumed by the mega cells which include estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells. The techniques of this application generate more accurate estimations of power consumption of integrated circuits than conventional techniques.

For example, independent claim 1 is directed to a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit. The method comprises (a) simulating logic of basic and mega cells of the integrated circuit, (b) estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells, (c)

estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the basic cells, and (d) combining the first and second values to obtain the power consumption of the integrated circuit.

Regarding the obviousness rejection based on Messerman as a primary reference, Applicants respectfully submit that the claims of this application cannot be obvious in view of a combination of references in which Messerman is the primary reference, since Messerman is not within the scope of the relevant art.

As pointed out above, the relevant art of this application is estimation of electric power consumption by integrated circuits which are comprised of basic cells and mega cells.

In contrast, Messerman is directed to extraction of a resistor network from an integrated circuit polygon layout. Operation of the resistor network is simulated to perform analysis of electromigration, the results of which can then be used to estimate the reliability of the integrated circuit.

The main problem to which Messerman is directed is stated by Messerman at column 1, lines 14-34 as follows:

> "Electromigration (EM) is the motion of ions through a conductor in response to the passage of current through the conductor. A divergence of ionic flux under the force of an "electron wind" may lead to the creation of vacancies, thus forming voids or holes in the conductor. The growth of the voids within a conductor may eventually lead to an open-circuit failure of the conductor. Accordingly, **electromigration is a serious and destructive wear out phenomenon**.
>
> Electromigration within the power supply circuitry (also termed the "power net") of an integrated circuit (IC) has serious consequences for the reliability of the IC, and also serves to reduce substantially the product life of the IC. The metal lines, vias, substrate taps and contacts which comprise the power net of an IC must all comply with predetermined electromigration design

> specifications to ensure the reliability of the IC. More specifically, the direct current flow through each fragment of the power net must be established, and compared to a predetermined maximum direct current threshold for the power net fragment in a process known as electromigration analysis."

Although Messerman is concerned with the problem of electromigration within a power net, there is no teaching, suggestion or other motivation in Messerman to apply any teachings of the reference towards estimation of power consumption by an integrated circuit. Since Messerman does not purport to be relevant to estimation of power consumption by an integrated circuit, one skilled in the art who is confronted with the problem of estimating power consumption by an integrated circuit would not have looked to Messerman as a starting point for the solution.

On the other hand, if one ignores the problem confronted by this application, and uses the claims as a roadmap for reconstructing the claimed invention, it may very well be that Messerman is equally likely to be selected in hindsight as any of several references in the universe of prior art, relevant or not. However, it is well-established that such hindsight reconstruction, for example, using a reference that falls outside of the scope of the relevant art, is impermissible.

The test of obviousness under 35 U.S.C. §103 is not whether all of the pieces of a claim can be found somewhere in the universe of prior art. Section 103 obviousness must be measured by a comparison of the claimed invention with the relevant art to determine the differences therebetween. Since Messerman is not relevant to estimation of power consumption by an integrated circuit, it simply cannot be the starting point of any permissible comparison between the

claimed invention and the relevant art.

The Office Action contends that the following single sentence in Messerman (at column 1, lines 34-45) renders the reference relevant to estimation of power consumption: "... Resistor networks are typically extended from the symbolic layout of an IC soley for the purpose of simulating the electrical characteristics of the IC."

It is noted that power consumption is not even mentioned in this cited sentence from Messerman (nor anywhere else in Messerman). Instead, the Office Action contends that the person skilled in the art would take an unguided leap to make a connection between the reference in Messerman to "electrical characteristics" on the one hand and estimating power consumption by an integrated circuit on the other hand, even though Messerman is expressly directed to the problem of electromigration and does not express a concern for power consumption. In order for the contention to have merit, the statement in Messerman of the problem confronted by the reference and the context of the reference, neither of which bears relation to estimation of power consumption by an integrated circuit, would have to be entirely ignored, and the cited statement would have to be placed in an entirely unsupported context.

In sum, Messerman, alone or considered along with the other cited references, does not provide teaching, suggestion or other motivation to render the claimed invention invalid.

Dangelo '678, as understood by Applicants, is directed to methodologies for deriving a valid structural description of a circuit or system (i.e. device) from a behavioral description thereof. According to the Office Action, Dangelo '678 teaches code for simulating logic of basic and mega cells of the integrated circuit.

Koza, as understood by Applicants, is directed to automated design of complex structures (such as circuits) using genetic algorithms. According to the Office Action, Koza discloses measuring alternating current of logic cells.

The Microsoft Press Computer Dictionary is cited in the Office Action as disclosing use of various computer readable media.

Applicants find no disclosure or suggestion by Dangelo '678, Koza and the Microsoft Press Computer Dictionary, alone or in combination, however, of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit, wherein the method comprises (a) estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells, (b) estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the basic cells, and (c) combining the first and second values to obtain the power consumption of the integrated circuit, as provided by the invention recited in independent claim 1 as amended.

Turning to the rejection based on a combination of Raman, Crafts and Dangelo '508, Raman, Crafts and Dangelo '508, like the other cited art, do not disclose or suggest the claimed invention.

Raman, as understood by Applicants, is directed to calculating current and power consumption of a circuit utilizing simulation and test vectors along with a model of the circuit. According to Raman, input test vectors are used to drive the model, and a simulator which operates the model maintains a toggle count for each device of the circuit. A characterization table is generated which contains an average switching current value of a type of a device for different values of capacitive loads. An activity factor can then be generated based on the number of the toggle count during a sample time period and the number of clock cycles during the sample period. Using the activity period, the current is determined from the average switching current for the device times the activity factor.

Applicants find no teaching or suggestion in Raman of several features of the claimed invention, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells.

Crafts, as understood by Applicants, is directed to calculation of dynamic power dissipation in CMOS circuits. According to Crafts, a determination is made of the capacitive load for each cell in a netlist for the CMOS circuit, from cell library data sheets. In addition, the capacitive loads of the interconnects between stages are estimated. A switching rate for each cell is then calculated, and the output frequency for the cell is determined. The power dissipation for each cell is calculated by multiplying the output frequency by the

capacitive load. The dynamic power dissipation for the circuit is determined by summing the power dissipation terms for each of the cells in the netlist.

Crafts was cited in the Office Action as purportedly disclosing calculating the alternating current component for each cell.

However, Applicants find no teaching or suggestion in Crafts of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells.

Dangelo '508, as understood by Applicants, is directed to generating structural descriptions of complex digital devices from high-level descriptions and specifications. Dangelo '508 was cited in the Office Action as purportedly disclosing use of mega cells and hardware description languages.

However, Applicants simply does not find teaching or suggestion in the cited art of estimating power consumption of an integrated circuit which includes estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells, as recited in independent claim 1.

Independent claims 9, 17, 25, 29, 33 and 37-39 are patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant

respectfully submits that independent claims 9, 17, 25, 29, 33 and 37-39, and the claims depending therefrom, are patentable over the cited art.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

The Office is hereby authorized to charge any additional fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,

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